

A

B

C

D

E

4

3

2

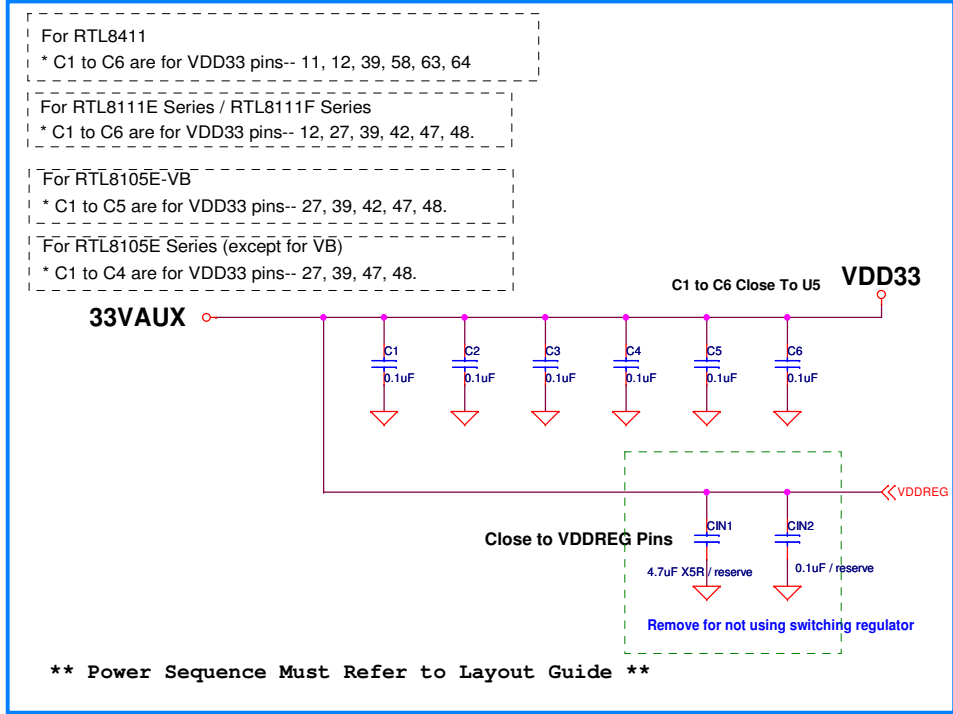
1

RTL8411/RTL8111E/RTL8111F/RTL8105E

64/48 Pin Reference Schematic V103

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2.	POWER
3.	QFN64 CONTROLLER
4.	QFN48 COLAY
5.	CARD READER
6.	OPTIONAL FUNCTION
7.	Change Notice

3.3V Power



Power-Supply Configuration Table

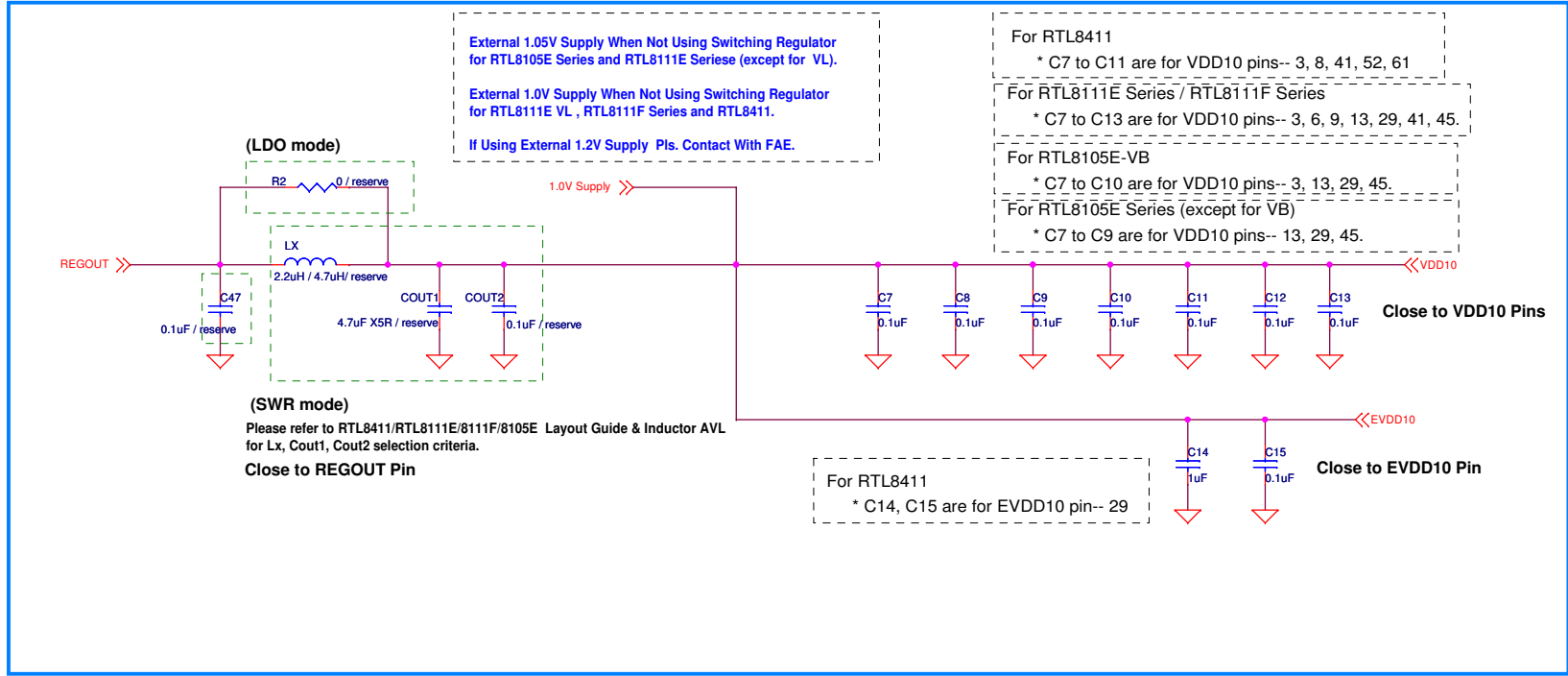
	mode	Cin1,2	R2	Lx	Cout1,2	R28	R31	C47
RTL8411/8111E Series/8111F Series/8105E Series	SWR	O	X	O	O	O	X	X
RTL8411	LDO	X	O	X	X	X	O	X
8105E Series(Expect for VB)	LDO	X	X	X	X	X	O	X
RTL8411	External	X	X	X	X	X	O	O
8105E Series (Except for VB)	External	X	X	X	X	O	X	X
RTL8111E Series/8111F Series/8105E-VB	External	X	X	X	X	X	O	X

If only one 1.05V / 1.0V supply source is selected for one PCB model, i.e. no other choices are reserved:

*** R28, R31 are not necessary. Just make a path of short to replace the use of R28/R31 on the table.

1. SWR mode only (8411/8111E series / 8111F series / 8105E series):
(2) R28 => short ENSWREG to VDD33.
(3) R31 => not necessary.
2. LDO mode only (8411/8105E series, except for VB):
(1) R28=> not necessary.
(2) R31 => short ENSWREG to GND
3. External supply only (8411/8111E series / 8111F series / 8105E-VB):
(1) R28 => not necessary.
(2) R31 => short ENSWREG to GND
4. External supply only (8105E Series, except for VB):
(1) R28 => short ENSWREG to VDD33.
(2) R31 => not necessary.

1.0V Power



SCL/LED CR R41 10K / reserve

TP1 LED1

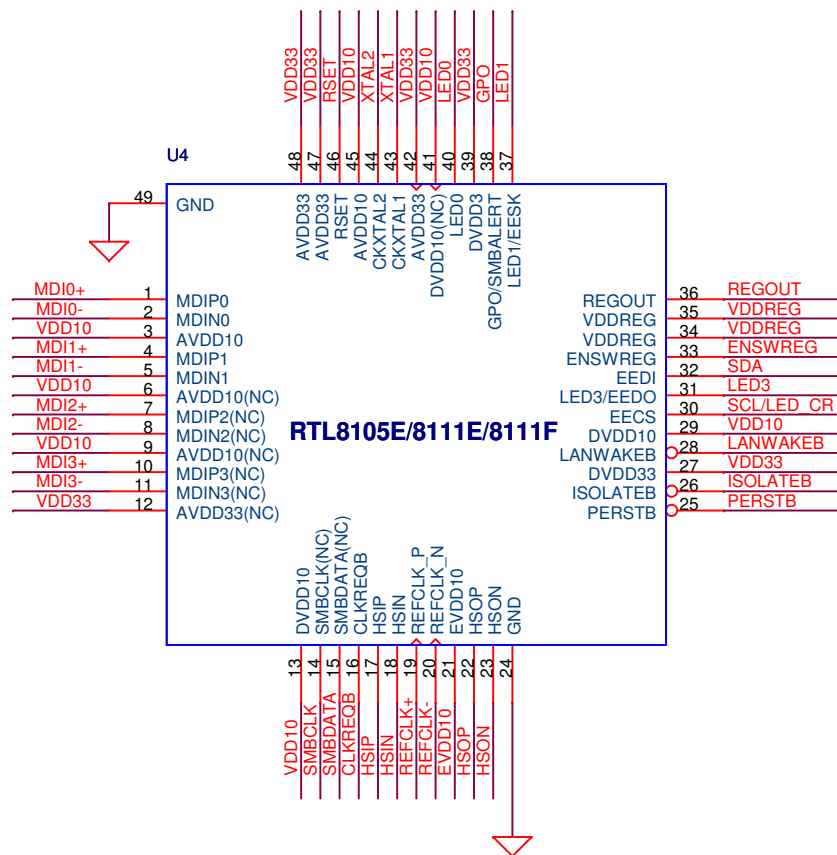
TP2 SDA

TP3 SCL/LED_CR

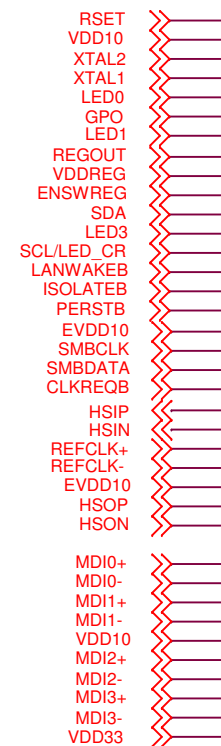
[illegible]

Diagram illustrating a 16-bit parallel adder structure. The inputs are SP1 and SP2, and the outputs are SP1 through SP16. The adder is composed of a series of full adders. The first full adder takes SP1[0] and SP2[0] as inputs and produces SP3[0] and a carry-out R16. Subsequent full adders take the next bits of SP1 and SP2, along with the carry-in from the previous stage (R17, R18, etc.), to produce the next output bit and carry-out. The final carry-out is R24.

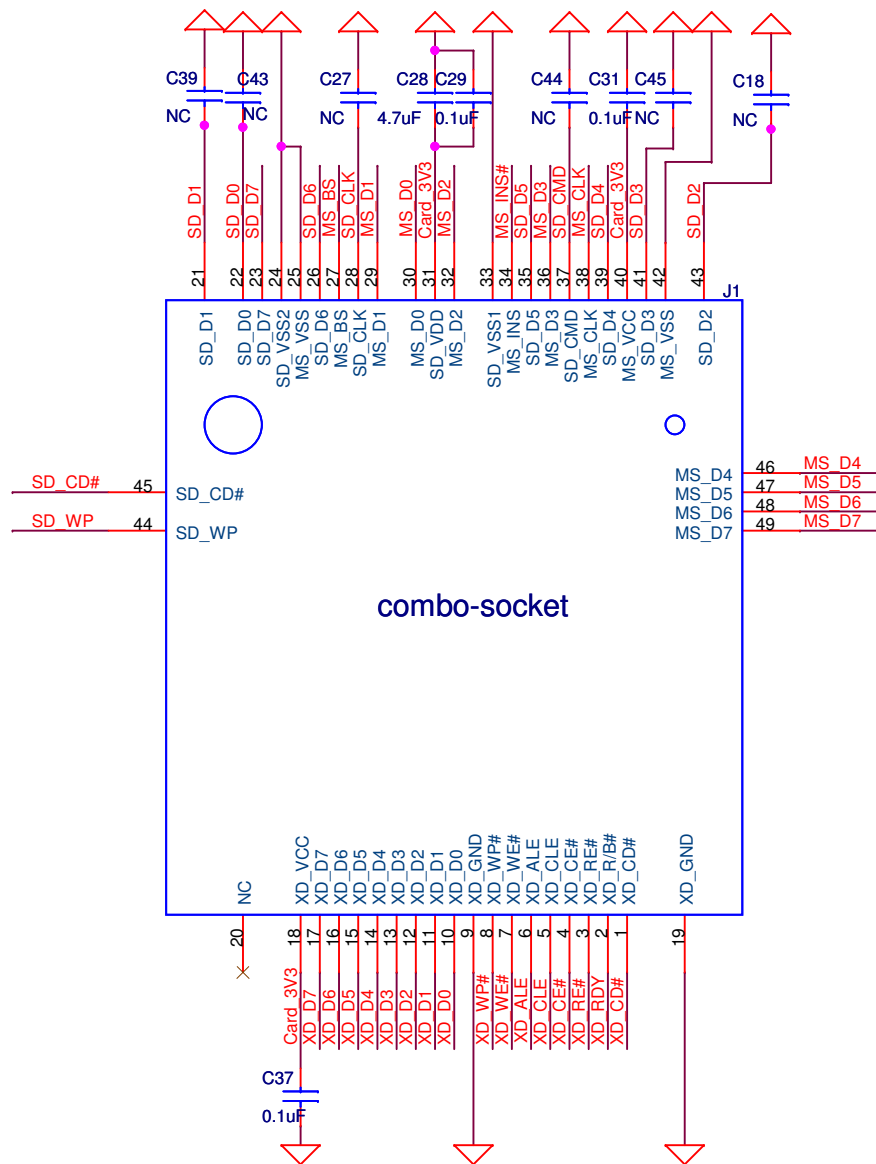
RTL8105E/8111E/8111F



RTL8411/8111 Colay



Card Reader

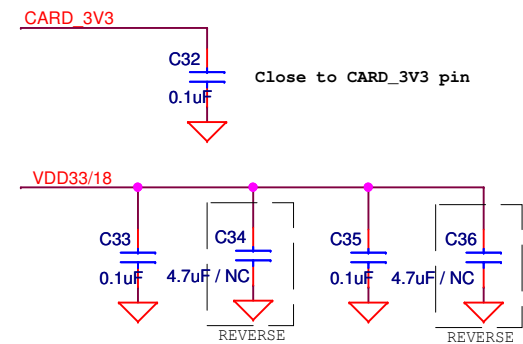


Flash Card Socket for reference

Share Pin

SP1	SD D7	xD RDY
SP2	SD D6	xD RE#
SP3	SD D5	xD CE#
SP4	SD D4	xD WE#
SP5	SD D1	xD D6
SP6	SD D0	xD D5
SP7	SD CLK	xD D4
SP8	SD CMD	xD D3
SP9	SD D3	xD D2
SP10	SD D2	xD D7
SP11	MS BS	xD CLE
SP12	SD WP	xD WP#
SP13	SD CD#	xD ALE
SP14	MS D4	xD D0
SP15	MS D0	xD D1
SP16		xD CD#

Power



For RTL8411

- *Place C33, C34 close to VDD33/18 pin -- 33
- *Place C35, C36 close to VDD33/18 pin -- 53

Realtek Semiconductor Corp.
No.2, Industry E. Rd. IX, Science-Based Industrial Park, Hsinchu, Taiwan 300

Title
RTL8411/8111E Reference Schematic : CARD READER

Size
A4

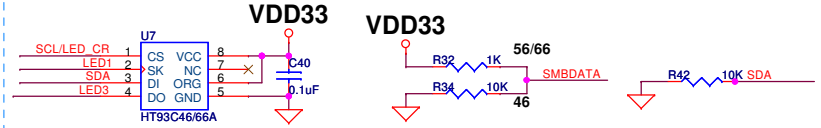
Document Number
RTL8411_8111E_REFERENCE_SCHEMATIC_V103.DSN

Rev
103

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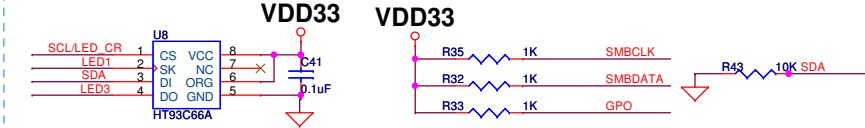
*** For RTL8111E Series and RTL8111F Series EEPROM / ASF Function (2 Option) ***

1. When using EEPROM only without ASF function.



Note: For RTL8111E-VL / RTL8111F, R32 must be 1K.
1. All components in this block will be needed only if an EEPROM is used without ASF function
Using R32 For 93C56/66
Using R34 For 93C46

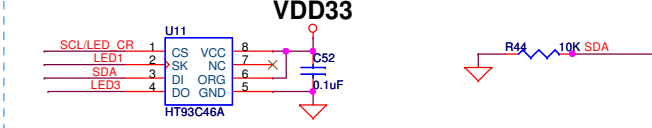
2. When using EEPROM (93C66) with ASF function



Note: This block is also for RTL8111E-VC using EEPROM_Less with ASF function.
1. All components in this block will be needed only if an EEPROM of 93C66 is used with ASF function

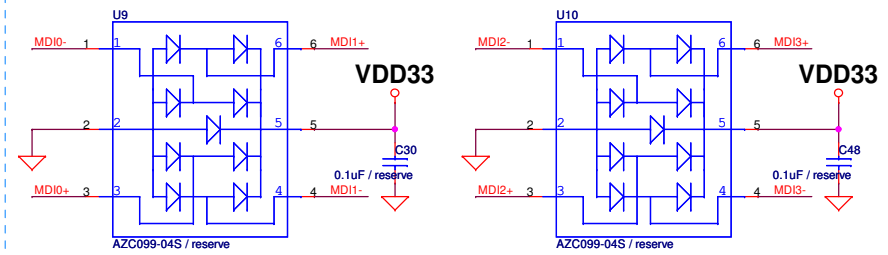
For RTL8105E Series EEPROM Function (1 Option)

1. When using EEPROM (93C46)



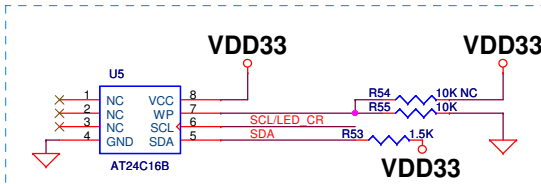
1. All components in this block will be needed only if an EEPROM of 93C46 is used

Reserved for TVS Components

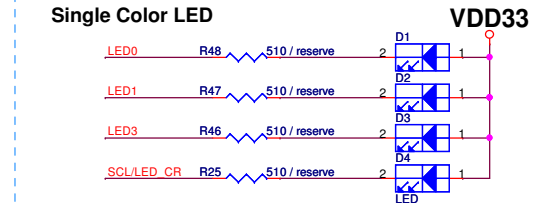


U9, U10 and C30, C48 are reserved for surge and cable ESD (Optional)

*** For RTL8411 Series TWSI Function (1 Option) ***



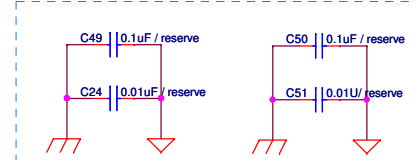
Optional LED Configuration



Support R>= 249 ohm resistor for Single Color LED.
Support R>= 125 ohm resistor for Dual Color LED.

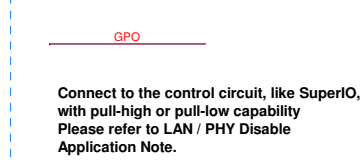
R25, R46, R47, R48 and D1, D2, D3, D4 Reserved for only Single Color LED Configuration (optional)

Reserved for Noise Isolation



C49, C24, C50, C51 Reserved for Noise Isolation between Chassis GND and System GND (optional)

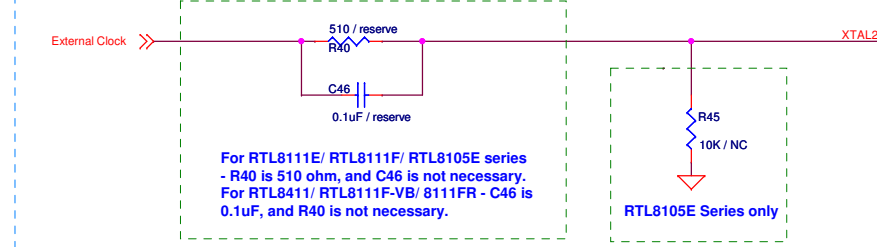
LAN/PHY Disable Function (Optional)



Reserved for Using External Clock Source

External 25MHz Clock

XTAL2 is external clock input pin.
XTAL1 must be floating when using oscillator or external clock.



External Clock Source Configuration Table

	R40	C46	R45
RTL8111E/ RTL8111F	O	X	X
RTL8411/ RTL8111F-VB	X	O	X
8105E Series	O	X	O

Change Notice from 1.00 to 1.01

- 1. Move all optional components to Page 6 (Optional Function)
- 2. Add Power selection guide to Page 2 (Power)
- 3. Add Test Point to page 3 (QFN64 Controller)
- 4. Remove Power On Latch on page 3 (QFN64 Controller)
- 5. Remove the block of Efuse-only in page 6 (Optional Function) for 8111E/8111F/8105E series
- 6. Modify QFN48 Colay QFN64 Line/Net Naming in Page 4 (QFN48 Colay)

Change Notice from 1.01 to 1.02

- 1.Modify Block of External Clock Source on Page 6.

Change Notice from 1.02 to 1.03

- 1.Revise for pin name in Page 3.

Title		
RTL8411/8111E Reference Schematic : Optional Function		
Size	Document Number	Rev
A	RTL8411_8111E_REFERENCE_SCHEMATIC_V103.DSN	103
Date:	Monday, August 06, 2012	Sheet 7 of 7