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RTL8111E Series

**INTEGRATED 10/100/1000M ETHERNET
CONTROLLER FOR PCI EXPRESS APPLICATIONS**

EEPROM-LESS APPLICATION NOTES

(CONFIDENTIAL: Development Partners Only)

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USING THIS DOCUMENT

This document is intended for the software engineer’s reference and provides detailed programming information.

Though every effort has been made to ensure that this document is current and accurate, more information may have become available subsequent to the production of this guide.

REVISION HISTORY

Revision	Release Date	Summary
1.0	2009/12/17	First release.
1.1	2010/05/26	Added the RTL8111E-VC-GR product number. Added section 8 ASF 2.0 Function Programming (RTL8111E-VC Only), page 10.
1.2	2010/08/05	Revised products covered by this document (now covers all RTL8111E products).
1.3	2010/10/04	Revised section 8 ASF 2.0 Function Programming (RTL8111E-VC Only), page 10.
1.4	2011/02/01	Revised 3 LAN MAC Address Programming, page 2.
1.5	2011/03/04	Minor revisions to section 8 ASF 2.0 Function Programming (RTL8111E-VC Only), page 10.
1.6	2012/05/18	Added section 5.2 RTL8111E-VL Only, page 6. Revised section 8 ASF 2.0 Function Programming (RTL8111E-VC Only), page 10. Added section 8.2 BIOS Setting Legacy Sensor Polling, page 12. Added section 8.3 BIOS Setting ASF Registers to Support ACPI Capability, page 13.
1.7	2012/08/13	Revised section 8 ASF 2.0 Function Programming (RTL8111E-VC Only), page 10.

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1. Introduction

This application note helps board designers to implement an EEPROM-less Realtek PCIe RTL8111E Series 10/100/1000M Ethernet board design. The interaction between the BIOS and driver are highlighted and discussed.

2. Design Considerations

Several major points must be considered when designing an EEPROM-less feature for Realtek's single chip PCIe RTL8111E Series 10/100/1000M Ethernet controller. Those points are listed below and are detailed in the following sections.

- LAN MAC Address Programming
- SID/SVID Programming (If Necessary)
- LED Mode Configuration
- Serial Number
- PXE Driver
- ASF 2.0 Function Programming (RTL8111E-VC Only)

3. LAN MAC Address Programming

3.1. RTL8111E Series (Excluding RTL8111E-VL)

Note: See section 3.2 for the RTL8111E-VL.

Due to the EEPROM-less design goal, the LAN MAC address cannot be loaded from EEPROM and stored in the RTL8111E Series. The BIOS must provide the MAC address to the RTL8111E Series each boot time. The RTL8111E Series will hold the MAC address until AC power is off (pulling the PCI reset low will not release the MAC address).

If the MAC address is 001122334455h:

Step1: Write C0h to I/O register offset 0x50 by byte access to disable ‘register protection’

Step2: Write 33221100h to I/O register offset 0x00 via double word access

Step3: Write 00005544h to I/O register offset 0x04 via double word access

Step4: Write 00h to I/O register offset 0x50 via byte access to enable ‘register protection’

Note: When the RTL8111E Series resumes from S3, S4, or S5, the BIOS must complete the steps given above.

3.2. RTL8111E-VL Only

If the MAC address is 001122334455h:

Step1: Write C0h to I/O register offset 0x50 by byte access to disable ‘register protection’

Step2: Write 33221100h to I/O register offset 0x00 via double word access

Step3: Write 00005544h to I/O register offset 0x04 via double word access

Step4: Write 11000000h to I/O register offset 0x70 via double word access

Step5: Write 8000F0F0h to I/O register offset 0x74 via double word access

Step6: Write 55443322h to I/O register offset 0x70 via double word access

Step7: Write 8000F0F4h to I/O register offset 0x74 via double word access

Step8: Write 00h to I/O register offset 0x50 via byte access to enable ‘register protection’

Note: When the RTL8111E-VL resumes from S3, S4, or S5, the BIOS must complete the steps given above.

4. SID/SVID Programming (If Necessary)

The default RTL8111E Series SID/SVID value is 8168/10EC. To change the value, follow the steps below:

If SID=8168h, SVID=10EC:

Step1: Write 816810EC to I/O register offset 0x64 via double word access

Step2: Write 8000F02Ch to I/O register offset 0x68 via double word access

Step3: Wait for 1ms

Note: When the RTL8111E Series resumes from S3, S4, or S5, the BIOS must complete the steps given above.

5. LED Mode Configuration

The RTL8111E Series supports three LED signals in four different configurable operation modes. The following sections describe the various LED actions. For LED configurations, refer to the related datasheet for details.

5.1. RTL8111E Series (Excluding RTL8111E-VL)

Note: See section 5.2, page 6 for the RTL8111E-VL LED operation mode.

5.1.1. Link Monitor

The Link Monitor senses link integrity, such as LINK₁₀, LINK₁₀₀, LINK₁₀₀₀, LINK_{10/100/1000}, LINK₁₀/ACT, LINK₁₀₀/ACT, or LINK₁₀₀₀/ACT. Whenever link status is established, the specific link LED pin is driven low. Once a cable is disconnected, the link LED pin is driven high, indicating that no network connection exists.

The LED_{S1~0} are I/O register 0x52 bit7:6.

Table 1. RTL8111E Series LEDs (Excluding RTL8111E-VL)

Symbol	Type	Pin No	Description				
LED0	O	40	LEDS1~0	00	01	10	11
			LED0	ACT _{ALL}	Link _{ALL} / ACT _{ALL}	Link ₁₀ / ACT _{ALL}	LINK ₁₀ / ACT ₁₀
LED1	O	37	LED1	LINK ₁₀₀	LINK ₁₀₀	LINK ₁₀₀	LINK ₁₀₀ / ACT ₁₀₀
LED3	O	31	LED3	LINK ₁₀₀₀	LINK ₁₀₀₀	LINK ₁₀₀₀	LINK ₁₀₀₀ / ACT ₁₀₀₀

Note 1: During power down mode, the LED signals are logic high.

Note 2: LED_{S1~0}'s initial value comes from the EEPROM. If there is no EEPROM, the default value of the (LED_{S1}, LED_{S0})=(1, 1).

5.1.2. RX LED

In 10/100/1000M mode, blinking of the RX LED indicates that receive activity is occurring.

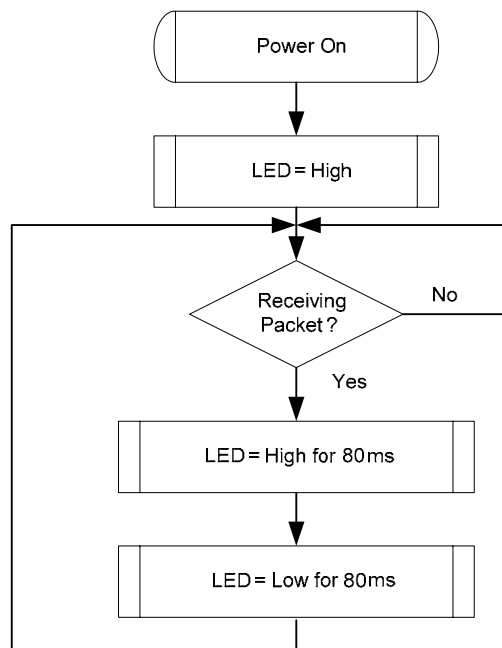


Figure 1. RX LED

5.1.3. TX LED

In 10/100/1000M mode, blinking of the TX LED indicates that transmit activity is occurring.

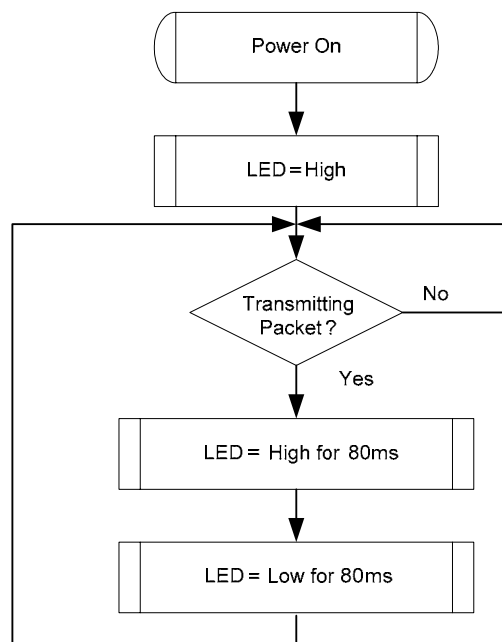


Figure 2. TX LED

5.1.4. LINK/ACT LED

In 10/100/1000M mode, blinking of the LINK/ACT LED indicates that the RTL8111E is linked and operating properly. When this LED is high for extended periods, it indicates that a link problem exists.

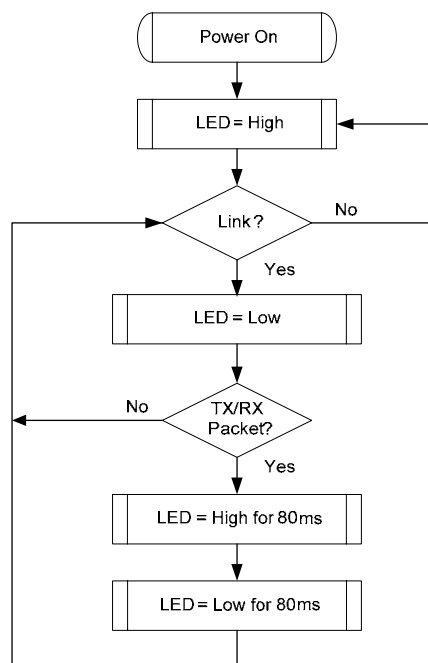


Figure 3. LINK/ACT LED

5.1.5. TX/RX LED

In 10/100/1000M mode, blinking of the TX/RX LED indicates that both transmit and receive activity is occurring.

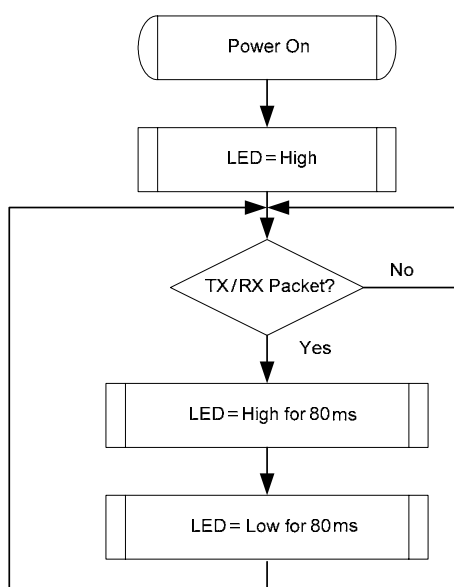


Figure 4. TX/RX LED

5.1.6. LED Mode Configuration

The default value of the RTL8111E LEDS1~0 is 11b. If the board layer designer wishes to change the value, please follow the steps below:

Step1: Write C0h to I/O register offset 0x50 via byte access to disable ‘register protection’

Step2: Write xx001111b to I/O register offset 0x52 via byte access (bit7 is LEDS1 and bit6 is LEDS0; refer to the datasheet to find which mode you need)

Step3: Write 00h to I/O register offset 0x50 via byte access to enable ‘register protection’

5.2. RTL8111E-VL Only

The RTL8111E-VL supports LED operation modes via IO register offset 18h~19h. Table 2 describes the different LED actions.

Table 2. LED Select (IO Register Offset 18h~19h) (RTL8111E-VL Only)

Bit	Symbol	RW	Description
15:12	LEDCntl	RW	LED Feature Control
11:8	LEDSEL3	RW	LED Select for PINLED3
7:4	LEDSEL1	RW	LED Select for PINLED1
3:0	LEDSEL0	RW	LED Select for PINLED0

When implementing customized LEDs:

Configure IO register offset 18h~19h to support your own LED signals. For example, if the value in the IO offset 0x18 is 0x0CA9h (0000110010101001b), the LED actions are:

- LED 0: On only in 10M mode, with blinking during TX/RX
- LED 1: On only in 100M mode, with blinking during TX/RX
- LED 3: On only in 1000M mode, with blinking during TX/RX

Table 3. Customized LEDs (RTL8111E-VL Only)

Speed	LINK			ACT/Full
	Link 10M	Link 100M	Link 1000M	
LED 0	Bit 0	Bit 1	Bit 2	Bit 3
LED 1	Bit 4	Bit 5	Bit 6	Bit 7
LED 3	Bit 8	Bit 9	Bit 10	Bit 11
Feature Control	Bit 12	Bit 13	Bit 14	Bit 15

Note: There are two special modes:

LED OFF Mode: Set all bits to 0. All LED pin outputs become floating (power saving).

Fixed LED Mode: Set Option 1 LED table Mode: LED0=LED1=LED3=1 or 2 (see Table 4).

Table 4. Fixed LED Mode (RTL8111E-VL Only)

Bit31~Bit0 Value	LED0	LED1	LED3
1XXX 0001 0001 0001	ACT	LINK	Full Duplex + Collision
1XXX 0010 0010 0010	Transmit	LINK	Receive

Note: ‘X’ indicates ‘irrelevant’.

Table 5. LED Feature Control-1 (RTL8111E-VL Only)

Feature Control	Bit12	Bit13	Bit14	Bit15
0	LED0 Low Active	LED1 Low Active	LED3 Low Active	Indicates Option 1 of Table 7 is selected
1	LED0 High Active	LED1 High Active	LED3 High Active	Indicates Option 2 of Table 7 is selected

Table 6. LED Feature Control-2 (RTL8111E-VL Only)

LED Pin	ACT=0	ACT=1
LINK=0	Floating	All Speed ACT
LINK>0	Selected Speed LINK	Option 1 (see Table 7): Selected Speed LINK+ Selected Speed ACT Option 2 (see Table 7): Selected Speed LINK+ All Speed ACT

Table 7. LED Option 1 & Option 2 Settings (RTL8111E-VL Only)

Link Bit			Active Bit	Description		
10	100	1000		Link	Option 1 LED Activity	Option 2 LED Activity
0	0	0	0	LED Off		
0	0	0	1	-	Act ₁₀ +Act ₁₀₀ +Act ₁₀₀₀	Act ₁₀ +Act ₁₀₀ +Act ₁₀₀₀
0	0	1	0	Link ₁₀₀₀	-	-
0	0	1	1	Link ₁₀₀₀	Act ₁₀₀₀	Act ₁₀ +Act ₁₀₀ +Act ₁₀₀₀
0	1	0	0	Link ₁₀₀	-	-
0	1	0	1	Link ₁₀₀	Act ₁₀₀	Act ₁₀ +Act ₁₀₀ +Act ₁₀₀₀
0	1	1	0	Link ₁₀₀ +Link ₁₀₀₀	-	-
0	1	1	1	Link ₁₀₀ +Link ₁₀₀₀	Act ₁₀₀ +Act ₁₀₀₀	Act ₁₀ +Act ₁₀₀ +Act ₁₀₀₀
1	0	0	0	Link ₁₀	-	-
1	0	0	1	Link ₁₀	Act ₁₀	Act ₁₀ +Act ₁₀₀ +Act ₁₀₀₀
1	0	1	0	Link ₁₀ +Link ₁₀₀₀	-	-
1	0	1	1	Link ₁₀ +Link ₁₀₀₀	Act ₁₀ +Act ₁₀₀₀	Act ₁₀ +Act ₁₀₀ +Act ₁₀₀₀
1	1	0	0	Link ₁₀ +Link ₁₀₀	-	-
1	1	0	1	Link ₁₀ +Link ₁₀₀	Act ₁₀ +Act ₁₀₀	Act ₁₀ +Act ₁₀₀ +Act ₁₀₀₀
1	1	1	0	Link ₁₀ +Link ₁₀₀ +Link ₁₀₀₀	-	-
1	1	1	1	Link ₁₀ +Link ₁₀₀ +Link ₁₀₀₀	Act ₁₀ +Act ₁₀₀ +Act ₁₀₀₀	Act ₁₀ +Act ₁₀₀ +Act ₁₀₀₀

Note:

Act₁₀ = LED blinking when Ethernet packets transmitted/received at 10Mbps.

Act₁₀₀ = LED blinking when Ethernet packets transmitted/received at 100Mbps.

Act₁₀₀₀ = LED blinking when Ethernet packets transmitted/received at 1000Mbps.

Link₁₀ = LED lit when Ethernet connection established at 10Mbps.

Link₁₀₀ = LED lit when Ethernet connection established at 100Mbps.

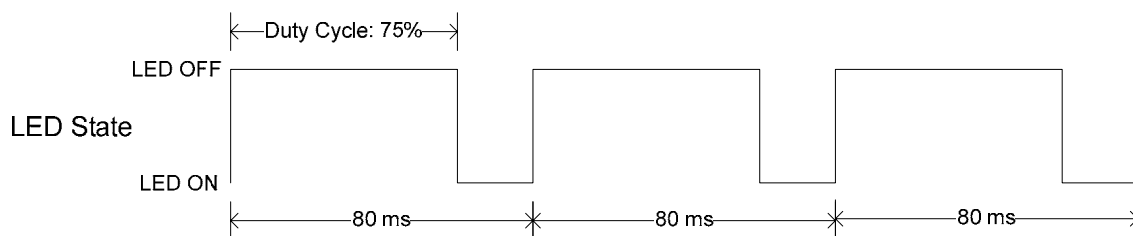
Link₁₀₀₀ = LED lit when Ethernet connection established at 1000Mbps.

5.2.1. LED Blinking Frequency Control (RTL8111E-VL Only)

The RTL8111E-VL supports LED blinking frequency control via IO register offset 1Ah to control user's LED blinking frequency and duty cycle (see Table 8). If the IO offset 0x1A is 0x0B (00001011b), the LED blinking frequency is 80ms and the duty cycle is 75%. The LED State is shown in Figure 5.

Table 8. LED Blinking Frequency Control (IO Offset 1Ah)

Bit	RW	Description
3:2	RW	LED Blinking Frequency 0: 240ms 1: 160ms (Default) 2: 80ms 3: Link Speed Dependent
1:0	RW	LED Blinking Duty Cycle 0: 12.5% 1: 25% 2: 50% (Default) 3: 75%



Note: Assumes the LED is low active.

Figure 5. LED Blinking Frequency Example

6. Serial Number

Due to the EEPROM-less design goal, the serial number cannot be loaded from EEPROM and stored in the RTL8111E. The BIOS must provide the serial number to the RTL8111E each boot time.

If the serial number is 00E04C6812345678h:

Step1: Write 684CE000h to I/O register offset 0x64 via double word access

Step2: Write 8000F164h to I/O register offset 0x68 via double word access

Step3: Wait for 1ms

Step4: Write 78563412h to I/O register offset 0x64 via double word access

Step5: Write 8000F168h to I/O register offset 0x68 via double word access

Step6: Wait for 1ms

Note: When the RTL8111E resumes from S3, S4, or S5, the BIOS must complete the steps given above.

7. PXE Driver

If the board layer designer wants to enable a Preboot Execution Environment (PXE) driver, the BIOS needs to write one byte of the PXE parameters in the I/O register 0xF0 to allow the ROM code to run properly. The default value of the PXE parameter is 00h (disable PXE). PXE parameter details are listed below.

Note: When the RTL8111E resumes from S3, S4, or S5, the BIOS must complete the steps given above.

Table 9. PXE Parameters

Bit	Symbol	RW	Description
7:6	Boot Protocol	RW	00: PXE protocol 01: RPL protocol
5:4	Boot order	RW	00: ROM disable 01: Int 18h 10: Int 19h 11: PnP/BEV (BBS)
3:0	-	-	Reserved

Note: When the EEPROM-less feature is implemented, the RTL8111E cannot WOL from '1st AC power-on'.

8. ASF 2.0 Function Programming (RTL8111E-VC Only)

The RTL8111E-VC supports the ASF 2.0 EEPROM-less feature via MAC Register Offset 0x70 (ERI Data Register) and 0x74 (ERI Address Register).

Before an ASF read/write the BIOS needs to enable the MAC register offset 0x50 Bit7=1, Bit6=1, 0x53 Bit6=1, Bit0=1, and 0x54 Bit7=1.

Write ASF Register Example 1 (Write 4-Byte Data):

Step1: Write the data (e.g., 0x12345678h) into the ERI Data Register (MAC Register Offset 0x70)

Step2: Write the address (e.g., 0x8002F010) into the ERI Address Register (MAC Register Offset 0x74)

The ERI Address Register then changes value from 0x8002F00A to 0x0002F010, and the data (0x12345678) is written into the ASF Register Offset 0x10

Note: 'F, 1111b' of 0x8002F010 sets Bit[15:12] of the ERI Address Register is DW (Double-Word) Byte Enabled.

For each bit of DW (Double-Word) Byte Enable field:

0b: Indicates that the corresponding byte of data must not be written into the mapped areas.

1b: Indicates that the corresponding byte of data must be written into the mapped areas.

Non-contiguous DW Byte Enable (enabled bytes separated by non-enabled bytes) are permitted. For example: 1010b, 0101b, 1001b, 1011b, 1101b.

The ASF address register should be DW aligned.

Write ASF Register Example 2 (Write 2-Byte Data):

Step1: Write the data (e.g., 0x1234) into the ERI Data Register (MAC Register Offset 0x70)

Step2: Write the address (e.g., 0x80023010) into the ERI Address Register (MAC Register Offset 0x74)

The ERI Address Register then changes value from 0x8002300A to 0x00023010, and the data (0x1234) is written into the ASF Register Offset 0x10.

Note: '3, 0011b' of 0x80023010 sets Bit[13:12] of the ERI Address Register and is DW (Double-Word) Byte Enabled.

For each bit of the DW (Double-Word) Byte Enables field:

0b: Indicates that the corresponding byte of data must not be written into the mapped areas.

1b: Indicates that the corresponding byte of data must be written into the mapped areas.

Non-contiguous DW Byte Enable (enabled bytes separated by non-enabled bytes) are permitted. For example: 1010b, 0101b, 1001b, 1011b, 1101b.

The ASF address register should be DW aligned.

Read ASF Register Example:

Step1: Write the address (0x0002F010) into the ERI Address Register (MAC Register Offset 0x74)

Step2: The ERI Address Register then changes value from 0x8002F010 to 0x8002F010

Step3: Read data from the ERI Data Register (MAC Register Offset 0x70), which is equal to the values in ASF Register Offset 0x10

8.1. ASF 2.0 Function Initialization Method

Step1: Write data (0x320014) to ASF Register Offset 0x000

Step2: Write data (0x0A040032) to ASF Register Offset 0x004

Step3: Write data (0x00C81E03) to ASF Register Offset 0x008

Step4: Write data (0x8B9B) to ASF Register Offset 0x00C

Step5: Write data (0x0000F867) to ASF Register Offset 0x088

Step6: Write data (0xF01F00) to ASF Register Offset 0x08C

Step7: Write data (0x00000400) to ASF Register Offset 0x118

Step8: Write data (0x00400000) to ASF Register Offset 0x11C

Step9: Write data (0xA200A200) to ASF Register Offset 0x224

Step10: Write data (see below) to ASF Register Offset 0x05E~0x069

INTEL: 88 00 03 88 00 02 88 00 01 88 00 04 (LSB~MSB)

AMD: 71 00 00 71 02 00 71 01 00 71 03 00 (LSB~MSB)

NVIDIA: E0 0A 00 E0 0A 02 E0 0A 01 E0 0A 03 (LSB~MSB)

Step11: Write UUID or GUID to ASF Register Offset 0x020~0x02F

Example: UUID = 00 11 22 33 44 55 66 77 88 99 AA BB CC DD EE FF (MSB~LSB)

Step12: Write SYSTEM_ID to ASF Register Offset 0x034~0x035

Example: SYSTEM_ID = 11 22 (MSB~LSB)

Step13: Write OPERATOR_KEY to ASF Register Offset 0x17C~0x18F

Example: OPERATOR_KEY = 98 73 F0 5B 1C 67 CC 50 D1 1E 2B B1 10 0D BB C3 8D D7 08 E2 (MSB~LSB)

Step14: Write ADMINISTRATOR_KEY to ASF Register Offset 0x190~0x1A3

Example: ADMINISTRATOR_KEY = 10 67 B4 D0 D5 2B C5 0C 3A AF 66 69 B7 34 45 99 28 F4 F9 CC (MSB~LSB)

Step15: Write GENERATOR_KEY to ASF Register Offset 0x1A4~0x1B7

Example: GENERATOR_KEY = DE EF 16 3B FB 8C 30 50 6B 3B F1 13 77 35 4D 9C 55 BD EB 87 (MSB~LSB)

Step16: Write CONSOLE_MAC_ADDRESS to Register Offset 0x010~0x015

Example: CONSOLE_MAC_ADDRESS = 00 E0 4C 68 00 01 (LSB~MSB)

Step17: Write CONSOLE_IP to ASF Register Offset 0x016~0x019

Example: CONSOLE_IP = C0 A8 00 0A (LSB~MSB)

Step18: Write CLINENT_IP to ASF Register Offset 0x01A~0x01D

Example: CLIENT_IP = C0 A8 00 01 (LSB~MSB)

Steps 13~18 are common user input values that are often changed. In addition to being directly filled by the BIOS, we recommend provision of a simple interface that will permit users to modify these steps without going through steps 1~12.

Note: When the RTL8111E resumes from S3, S4, or S5, the BIOS must complete Steps 1~18 above. If the ASF Register is changed by the user from the BIOS interface, to avoid register values being cleared by power on reset the corresponding storage device should be updated immediately.

8.2. BIOS Setting Legacy Sensor Polling

Step1: Write data (0x01~0x08) to ASF Register Offset 0xAD for setting the number of legacy sensor devices

Step2: Write data (see the table note below) to ASF Register Offset 0xB0~0xBA

Table 10. BIOS Setting Legacy Sensor Polling

Offset	Symbol	RW	Description						
0x00B0 (1B)	LSnsrAddr	RW	SMBus Address of Legacy Sensor An SMBus address of 0x00 means no other legacy SMBus sensors.						
			<table><tr><th>Bit(s)</th><th>Description</th></tr><tr><td>7:1</td><td>Contains the SMBus address of the legacy sensor device.</td></tr><tr><td>0</td><td>Identifies whether (1) or not (0) the alerting condition (event) is based on an exact match.</td></tr></table>	Bit(s)	Description	7:1	Contains the SMBus address of the legacy sensor device.	0	Identifies whether (1) or not (0) the alerting condition (event) is based on an exact match.
			Bit(s)	Description					
			7:1	Contains the SMBus address of the legacy sensor device.					
0	Identifies whether (1) or not (0) the alerting condition (event) is based on an exact match.								
0x00B1 (1B)	LAlertCMD	RW	Legacy Alert Command Contains the SMBus command or register value used to obtain the data associated with the event.						
0x00B2 (1B)	LAlertDataMsk	RW	Legacy Alert Data Mask The data-mask to be logically AND'd with the returned sensor data to isolate significant bits associated with this event.						
0x00B3 (1B)	LAlertCmp	RW	Legacy Alert Compare Value The value to compare to the masked sensor data, if an exact match is specified in the Device Address field. If a match results, the alert associated with this event should be sent by the alert-sending device.						
0x00B4 (1B)	LAlertESnsrT	RW	Legacy Alert Event Sensor Type						
0x00B5 (1B)	LAlertET	RW	Legacy Alert Event Type						
0x00B6 (1B)	LAlertEOffset	RW	Legacy Alert Event Offset The value specified here by the system's firmware always has bit7 set to 0b to indicate that the alert information is associated with an event assertion.						
0x00B7 (1B)	LAlertES	RW	Legacy Alert Event Severity						
0x00B8 (1B)	LAlertSN	RW	Legacy Alert Sensor Number						
0x00B9 (1B)	LAlertEntity	RW	Legacy Alert Entity						
0x00BA (1B)	LAlertEI	RW	Legacy Alert Entity Instance						

Note:

Set values of ASF Register Offset 0xB0~0xBA for legacy sensor device 0.

Set values of ASF Register Offset 0xBD~0xC7 for legacy sensor device 1.

Set values of ASF Register Offset 0xCA~0xD4 for legacy sensor device 2.

Set values of ASF Register Offset 0xD7~0xE1 for legacy sensor device 3.

Set values of ASF Register Offset 0xE4~0xEE for legacy sensor device 4.

Set values of ASF Register Offset 0xF1~0xFB for legacy sensor device 5.

Set values of ASF Register Offset 0xFE~0x108 for legacy sensor device 6.

Set values of ASF Register Offset 0x10B~0x115 for legacy sensor device 7.

Step3: After setting all legacy sensor devices, write data (0xAB) to ASF Register Offset 0x0D

8.3. BIOS Setting ASF Registers to Support ACPI Capability

Step1: Write data (depends on ACPI Table contents) to ASF Register Offset 0x050~0x053

Table 11. BIOS Setting ASF Registers to Support ACPI Capability-1

Offset	Symbol	RW	Description	
0x0050~0x0053 (4B)	FmCapMsk	RW	System Firmware Capabilities Bit Mask (for Administrator)	
			Bit	Description
			Bit 31:16	Reserved for future definition by this specification
			Bit 15	Supports Configuration Data Reset, if set to 1b
			Bit 14	Supports Firmware Verbosity/Quiet, if set to 1b
			Bit 13	Supports Firmware Verbosity/Verbose, if set to 1b
			Bit 12	Supports Forced Progress Events, if set to 1b
			Bit 11	Supports User Password Bypass, if set to 1b
			Bit 10:7	Reserved for future definition by this specification
			Bit 6	Supports Sleep Button Lock, if set to 1b
			Bit 5	Supports Lock Keyboard, if set to 1b
			Bit 4:3	Reserved for future definition by this specification, set to 00b
			Bit 2	Supports Reset Button Lock, if set to 1b
			Bit 1	Supports Power Button Lock, if set to 1b
Bit 0	Supports Firmware Verbosity/Screen Blank, if set to 1b			

Step2: Write data (depends on ACPI Table contents) to ASF Register Offset 0x054~0x056

Table 12. BIOS Setting ASF Registers to Support ACPI Capability-2

Offset	Symbol	RW	Description	
0x0054~0x0055 (2B)	SpCMDMsk	RW	Special Commands Bit Mask (for Administrator)	
			Bit	Description
			Bit 15:13	Reserved to identify support for ASF-RMCP Special Commands, defined by a future version of this specification, set to 000b
			Bit 12	Supports Force CD/DVD Boot command, if set to 1b
			Bit 11	Supports Force Diagnostic Boot command, if set to 1b
			Bit 10	Supports Force Hard-drive Safe-mode Boot command, if set to 1b
			Bit 9	Supports Force Hard-drive Boot command, if set to 1b
			Bit 8	Supports Force PXE Boot command, if set to 1b
			Bit 7:0	Reserved to identify support for ASF-RMCP Special Commands, defined by a future version of this specification, set to 00h

Offset	Symbol	RW	Description	
0x0056 (1B)	SysCapMsk	RW	System Capabilities Bit Mask (for Administrator)	
			Bit	Description
			Bit 7	Supports Reset on either the compatibility or secure port, if set to 1b
			Bit 6	Supports Power-Up on either the compatibility or secure port, if set to 1b
			Bit 5	Supports Power-Down on either the compatibility or secure port, if set to 1b
			Bit 4	Supports Power Cycle Reset on either the compatibility or secure port, if set to 1b
			Bit 3	Supports Reset only on the secure port, if set to 1b
			Bit 2	Supports Power-Up only on the secure port, if set to 1b
			Bit 1	Supports Power-Down only on the secure port, if set to 1b
			Bit 0	Supports Power Cycle Reset only on the secure port, if set to 1b

Step3: Write data (depends on ACPI Table contents) ASF Register Offset 0x088~0x08B

Table 13. BIOS Setting ASF Registers to Support ACPI Capability-3

Offset	Symbol	RW	Description	
0x0088~0x008B (4B)	FmCapMsk	RW	System Firmware Capabilities Bit Mask (for Operator)	
			Bit	Description
			Bit 31:16	Reserved for future definition by this specification
			Bit 15	Supports Configuration Data Reset, if set to 1b
			Bit 14	Supports Firmware Verbosity/Quiet, if set to 1b
			Bit 13	Supports Firmware Verbosity/Verbose, if set to 1b
			Bit 12	Supports Forced Progress Events, if set to 1b
			Bit 11	Supports User Password Bypass, if set to 1b
			Bit 10:7	Reserved for future definition by this specification
			Bit 6	Supports Sleep Button Lock, if set to 1b
			Bit 5	Supports Lock Keyboard, if set to 1b
			Bit 4:3	Reserved for future definition by this specification, set to 00b.
			Bit 2	Supports Reset Button Lock, if set to 1b
			Bit 1	Supports Power Button Lock, if set to 1b
			Bit 0	Supports Firmware Verbosity/Screen Blank, if set to 1b

Step4: Write data (depends on ACPI Table contents) ASF Register Offset 0x08C~0x08E

Table 14. BIOS Setting ASF Registers to Support ACPI Capability-4

Offset	Symbol	RW	Description	
0x008C~0x008D (2B)	SpCMDMsk	RW	Special Commands Bit Mask (for Operator)	
			Bit	Description
			Bit 15:13	Reserved to identify support for ASF-RMCP Special Commands, defined by a future version of this specification, set to 000b.
			Bit 12	Supports Force CD/DVD Boot command, if set to 1b.
			Bit 11	Supports Force Diagnostic Boot command, if set to 1b.
			Bit 10	Supports Force Hard-drive Safe-mode Boot command, if set to 1b.
			Bit 9	Supports Force Hard-drive Boot command, if set to 1b.
			Bit 8	Supports Force PXE Boot command, if set to 1b.
Bit 7:0	Reserved to identify support for ASF-RMCP Special Commands, defined by a future version of this specification, set to 00h.			
0x008E (1B)	SysCapMsk	RW	System Capabilities Bit Mask (for Operator)	
			Bit	Description
			Bit 7	Supports Reset on either the compatibility or secure port, if set to 1b
			Bit 6	Supports Power-Up on either the compatibility or secure port, if set to 1b
			Bit 5	Supports Power-Down on either the compatibility or secure port, if set to 1b
			Bit 4	Supports Power Cycle Reset on either the compatibility or secure port, if set to 1b
			Bit 3	Supports Reset only on the secure port, if set to 1b.
			Bit 2	Supports Power-Up only on the secure port, if set to 1b.
			Bit 1	Supports Power-Down only on the secure port, if set to 1b.
			Bit 0	Supports Power Cycle Reset only on the secure port, if set to 1b.

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