

REALTEK

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RTL8111E Series

**INTEGRATED GIGABIT ETHERNET CONTROLLER
FOR PCI EXPRESS APPLICATIONS**

EEPROM-LESS APPLICATION NOTES
(CONFIDENTIAL: Development Partners Only)

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USING THIS DOCUMENT

This document is intended for the software engineer’s reference and provides detailed programming information.

Though every effort has been made to ensure that this document is current and accurate, more information may have become available subsequent to the production of this guide.

REVISION HISTORY

Revision	Release Date	Summary
1.0	2009/12/17	First release.
1.1	2010/05/26	Added the RTL8111E-VC-GR product number. Added section 8 ASF 2.0 Function Programming (RTL8111E-VC Series Only), page 7.
1.2	2010/08/05	Revised products covered by this document (now covers all RTL8111E products).
1.3	2010/10/04	Added section 8 ASF 2.0 Function Programming (RTL8111E-VC Series Only), page 7.

Table of Contents

1.	INTRODUCTION	1
2.	DESIGN CONSIDERATIONS.....	1
3.	LAN MAC ADDRESS PROGRAMMING.....	1
4.	SID/SVID PROGRAMMING (IF NECESSARY)	2
5.	LED MODE CONFIGURATION	2
5.1.	LINK MONITOR	2
5.2.	RX LED.....	3
5.3.	TX LED.....	3
5.4.	LINK/ACT LED.....	4
5.5.	TX/RX LED	5
5.6.	LED MODE CONFIGURATION.....	5
6.	SERIAL NUMBER.....	6
7.	PXE DRIVER.....	6
8.	ASF 2.0 FUNCTION PROGRAMMING (RTL8111E-VC SERIES ONLY)	7

List of Tables

TABLE 1.	LEDS	2
TABLE 2.	PXE PARAMETERS.....	6

List of Figures

FIGURE 1.	RX LED	3
FIGURE 2.	TX LED	3
FIGURE 3.	LINK/ACT LED	4
FIGURE 4.	TX/RX LED.....	5

1. Introduction

This application note helps board designers to implement an EEPROM-less Realtek PCI-E RTL8111E Series gigabit Ethernet board design. The interaction between the BIOS and driver are highlighted and discussed.

2. Design Considerations

Several major points must be considered when designing an EEPROM-less feature for Realtek's single chip PCI-E RTL8111E gigabit Ethernet controller. Those points are listed below and are detailed in the following sections.

- LAN MAC Address Programming
- SID/SVID Programming (If Necessary)
- LED Mode Configuration
- Serial Number
- PXE Driver
- ASF 2.0 Function Programming (RTL8111E-VC series Only)

3. LAN MAC Address Programming

Due to the EEPROM-less design goal, the LAN MAC address cannot be loaded from EEPROM and stored in the RTL8111E. The BIOS must provide the MAC address to the RTL8111E each boot time. The RTL8111E will hold the MAC address until AC power is off (pulling the PCI reset low will not release the MAC address).

If the MAC address is 001122334455h:

Step1: Write C0h to I/O register offset 0x50 by byte access to disable 'register protection'

Step2: Write 33221100h to I/O register offset 0x00 via double word access

Step3: Write 00005544h to I/O register offset 0x04 via double word access

Step4: Write 00h to I/O register offset 0x50 via byte access to enable 'register protection'

Note: When the RTL8111E resumes from S3, S4, or S5, the BIOS must complete the steps given above.

4. SID/SVID Programming (If Necessary)

The default RTL8111E SID/SVID value is 8168/10EC. If the board layer designer wants to change the value, please follow the steps below:

If SID=8168h, SVID=10EC:

Step1: Write 816810EC to I/O register offset 0x64 via double word access

Step2: Write 8000F02Ch to I/O register offset 0x68 via double word access

Step3: Wait for 1ms

Note: When the RTL8111E resumes from S3, S4, or S5, the BIOS must complete the steps given above.

5. LED Mode Configuration

The RTL8111E supports three LED signals in four different configurable operation modes. The following sections describe the various LED actions.

5.1. Link Monitor

The Link Monitor senses link integrity, such as LINK10, LINK100, LINK1000, LINK10/100/1000, LINK10/ACT, LINK100/ACT, or LINK1000/ACT. Whenever link status is established, the specific link LED pin is driven low. Once a cable is disconnected, the link LED pin is driven high, indicating that no network connection exists. The LED_{S1~0} are I/O register 0x52 bit_{7:6}.

Table 1. LEDs

Symbol	Type	Pin No	Description				
LED0	O	40	LED _{S1~0}	00	01	10	11
			LED0	ACT _{ALL}	Link _{ALL} / ACT _{ALL}	Link10/ ACT _{ALLX}	LINK10/ ACT ₁₀
LED1	O	37	LED1	LINK100	LINK100	LINK100	LINK100/ ACT ₁₀₀
LED3	O	31	LED3	LINK1000	LINK1000	LINK1000	LINK1000/ ACT ₁₀₀₀

Note 1: During power down mode, the LED signals are logic high.

Note 2: LED_{S1~0}'s initial value comes from the EEPROM. If there is no EEPROM, the default value of the (LED_{S1}, LED_{S0})=(1, 1).

5.2. ***RX LED***

In 10/100/1000Mbps mode, blinking of the RX LED indicates that receive activity is occurring.

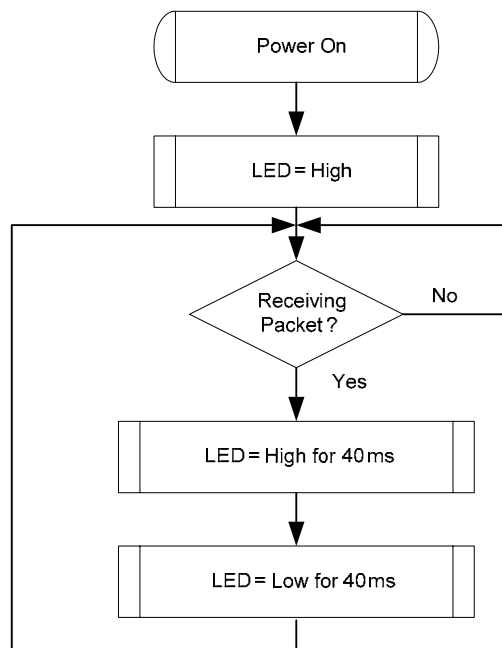


Figure 1. RX LED

5.3. ***TX LED***

In 10/100/1000Mbps mode, blinking of the TX LED indicates that transmit activity is occurring.

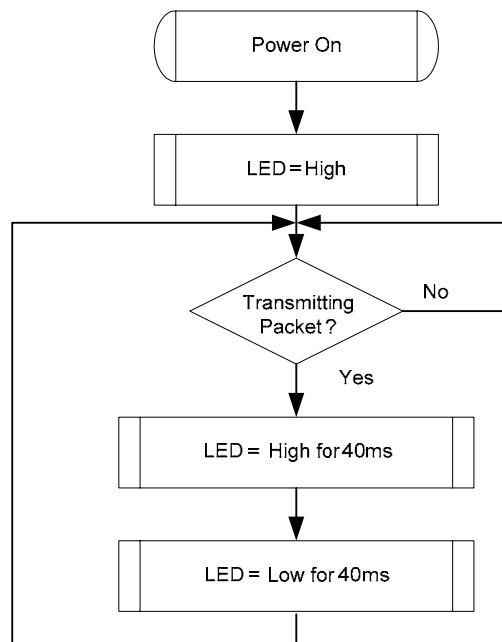


Figure 2. TX LED

5.4. *LINK/ACT LED*

In 10/100/1000Mbps mode, blinking of the LINK/ACT LED indicates that the RTL8111E is linked and operating properly. When this LED is high for extended periods, it indicates that a link problem exists.

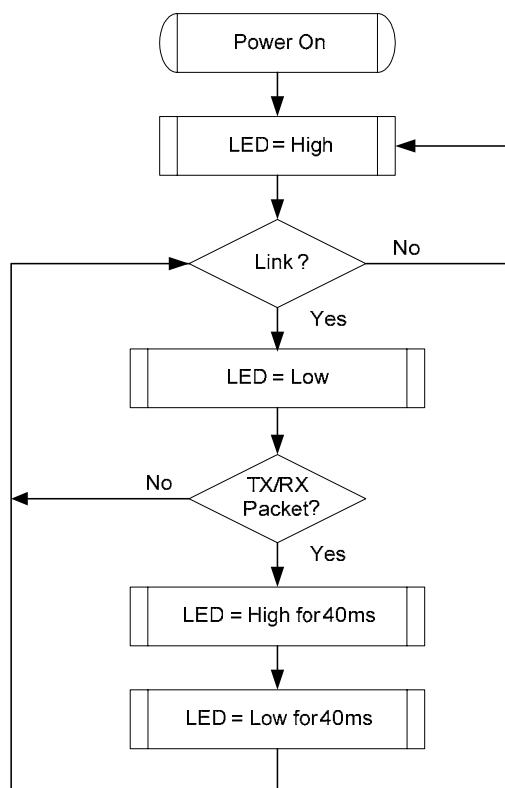


Figure 3. LINK/ACT LED

5.5. TX/RX LED

In 10/100/1000Mbps mode, blinking of the TX/RX LED indicates that both transmit and receive activity is occurring.

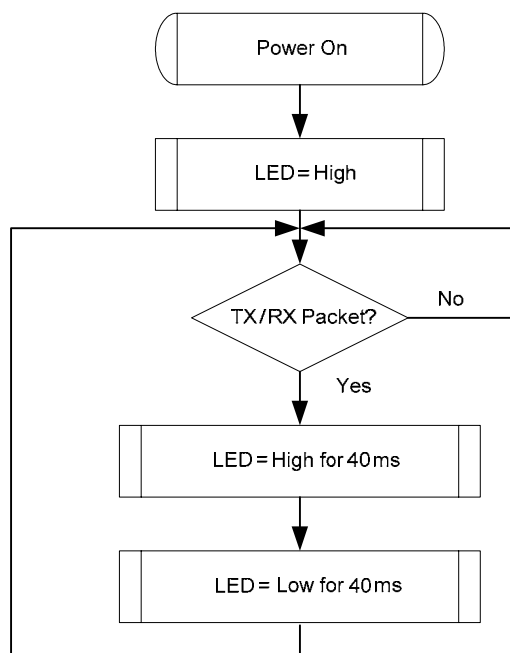


Figure 4. TX/RX LED

5.6. LED Mode Configuration

The default value of the RTL8111E LEDS1~0 is 11b. If the board layer designer wishes to change the value, please follow the steps below:

Step1: Write C0h to I/O register offset 0x50 via byte access to disable 'register protection'.

Step2: Write xx001111b to I/O register offset 0x52 via byte access (bit7 is LEDS1 and bit6 is LEDS0; refer to the datasheet to find which mode you need).

Step3: Write 00h to I/O register offset 0x50 via byte access to enable 'register protection'.

6. Serial Number

Due to the EEPROM-less design goal, the serial number cannot be loaded from EEPROM and stored in the RTL8111E. The BIOS must provide the serial number to the RTL8111E each boot time.

If the serial number is 00E04C6812345678h:

Step1: Write 684CE000h to I/O register offset 0x64 via double word access.

Step2: Write 8000F164h to I/O register offset 0x68 via double word access.

Step3: Wait for 1ms.

Step4: Write 78563412h to I/O register offset 0x64 via double word access.

Step5: Write 8000F168h to I/O register offset 0x68 via double word access.

Step6: Wait for 1ms.

Note: When the RTL8111E resumes from S3, S4, or S5, the BIOS must complete the steps given above.

7. PXE Driver

If the board layer designer wants to enable a Preboot Execution Environment (PXE) driver, the BIOS needs to write one byte of the PXE parameters in the I/O register 0xF0 to allow the ROM code to run properly. The default value of the PXE parameter is 00h (disable PXE). PXE parameter details are listed below.

Note: When the RTL8111E resumes from S3, S4, or S5, the BIOS must complete the steps given above.

Table 2. PXE Parameters

Bit	Symbol	RW	Description
7:6	Boot Protocol	RW	00: PXE protocol 01: RPL protocol
5:4	Boot order	RW	00: ROM disable 01: Int 18h 10: Int 19h 11: PnP/BEV (BBS)
3:0	-	-	Reserved

Note: When the EEPROM-less feature is implemented, the RTL8111E cannot WOL from '1st AC power-on'.

8. ASF 2.0 Function Programming (RTL8111E-VC Series Only)

The RTL8111E-VC series supports the ASF 2.0 EEPROM-less feature via MAC Register Offset 0x70 (ERI Data Register) and 0x74 (ERI Address Register).

Before an ASF read/write the BIOS needs to enable the MAC register offset 0x50 Bit7=1, Bit6=1, 0x53 Bit6=1, Bit0=1, and 0x54 Bit7=1.

Write ASF Register Example:

Step1: Write the data (0x12345678h) into the ERI Data Register (MAC Register Offset 0x70)

Step2: Write the address (0x8002F00A) into the ERI Address Register (MAC Register Offset 0x74)

Step3: The ERI Address Register then changes value from 0x8002F00A to 0x0002F00A, and the data (0x12345678) is written into the ASF Register Offset 0x0A

Read ASF Register Example:

Step1: Write the address (0x0002F00A) into the ERI Address Register (MAC Register Offset 0x74)

Step2: The ERI Address Register then changes value from 0x0002F00A to 0x8002F00A

Step3: Read data from the ERI Data Register (MAC Register Offset 0x70), which is equal to the values in ASF Register Offset 0x0A

ASF 2.0 Function Initialization Method:

Step1: Write data (0x00320014) to ASF Register Offset 0x000

Step2: Write data (0x0A040032) to ASF Register Offset 0x004

Step3: Write data (0x00C81E03) to ASF Register Offset 0x008

Step4: Write data (0x00008B9B) to ASF Register Offset 0x00C

Step5: Write data (0x0000F867) to ASF Register Offset 0x088

Step6: Write data (0x0EF01F00) to ASF Register Offset 0x08C

Step7: Write data (0x00000400) to ASF Register Offset 0x118

Step8: Write data (0x00400000) to ASF Register Offset 0x11C

Step9: Write data (0xA200A200) to ASF Register Offset 0x224

Step10: Write data (see below, LSB~MSB) to ASF Register Offset 0x05E~0x069

INTEL: 88 00 03 88 00 02 88 00 01 88 00 04

AMD: 71 00 00 71 02 00 71 01 00 71 03 00

NVIDIA: E0 0A 00 E0 0A 02 E0 0A 01 E0 0A 03

Step11: Write UUID or GUID (MSB~LSB) to ASF Register Offset 0x020~0x02F

Example: UUID = 00 11 22 33 44 55 66 77 88 99 AA BB CC DD EE FF

Step12: Write SYSTEM_ID (MSB~LSB) to ASF Register Offset 0x034~0x035

Example: SYSTEM_ID = 11 22

Step13: Write OPERATOR_KEY (MSB~LSB) to ASF Register Offset 0x17C~0x18F

Example: OPERATOR_KEY = 98 73 F0 5B 1C 67 CC 50 D1 1E 2B B1 10 0D BB C3 8D D7 08 E2

Step14: Write ADMINISTRATOR_KEY (MSB~LSB) to ASF Register Offset 0x190~0x1A3

Example: ADMINISTRATOR_KEY = 10 67 B4 D0 D5 2B C5 0C 3A AF 66 69 B7 34 45 99 28 F4 F9 CC

Step15: Write GENERATOR_KEY (MSB~LSB) to ASF Register Offset 0x1A4~0x1B7

Example: GENERATOR_KEY = DE EF 16 3B FB 8C 30 50 6B 3B F1 13 77 35 4D 9C 55 BD EB 87

Step16: Write CONSOLE_MAC_ADDRESS (LSB~MSB) to Register Offset 0x010~0x015

Example: CONSOLE_MAC_ADDRESS = 00 E0 4C 68 00 01

Step17: Write CONSOLE_IP (MSB~LSB) to ASF Register Offset 0x016~0x019

Example: CONSOLE_IP = C0 A8 00 0A

Step18: Write CLINENT_IP (MSB~LSB) to ASF Register Offset 0x01A~0x01D

Example: CLIENT_IP = C0 A8 00 01

Steps 13~18 are common user input values that are often changed. In addition to being directly filled by the BIOS, we recommend provision of a simple interface that will permits users to modify these steps without going through steps 1~12.

Note: When the RTL8111E resumes from S3, S4, or S5, the BIOS must complete Steps 1~18 above.

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