

REALTEK

ETHERNET CONTROLLER DEEP SLUMBER MODE (DSM)

APPLICATION NOTES (CONFIDENTIAL: Development Partners Only)

Rev. 1.92

31 August 2009

Track ID: TVER-1076-21



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USING THIS DOCUMENT

This document is intended for the engineer’s reference and provides detailed application information.

Though every effort has been made to ensure that this document is current and accurate, more information may have become available subsequent to the production of this guide.

REVISION HISTORY

Revision	Release Date	Summary
1.0	2007/05/19	First release.
1.1	2007/08/18	Revised section 2 Deep Slumber Mode Version 1 (DSMv1), page 1. Revised Figure 1, page 2, and Figure 5, page 4. Revised section 5 Power Consumption, page 9.
1.2	2008/02/01	Revised section 2 Deep Slumber Mode Version 1 (DSMv1), page 1.
1.3	2008/06/06	Added section 4 ACPI RMV, page 8.
1.4	2008/10/03	Added Figure 3, page 3. Revised section 5 Power Consumption, page 9.
1.5	2008/10/29	Added RTL8103E figure (Figure 2, page 3). Added Table 4 RTL8103E & RTL8103T Power Consumption, page 9.
1.6	2008/12/22	Added RTL8103T data.
1.7	2009/03/23	Added Deep Slumber Mode version 2 (DSMv2) information. Revised section 4 ACPI RMV, page 8. Revised section 5.2 RTL8111D(L) Power Consumption, page 9. Added section 5.3 RTL8111D(L)-VB Power Consumption, page 9. Added section 5.5 RTL8103E(L)-VB & RTL8103T-VB Power Consumption, page 10.
1.8	2009/04/03	Corrected minor typing errors.
1.9	2009/04/08	Revised driver revision Note 6, page 6.
1.91	2009/06/15	Revised driver revision Note 6, page 6. Revised section 5.5 RTL8103E(L)-VB & RTL8103T-VB Power Consumption, page 10.
1.92	2009/08/31	Revised section 3 Deep Slumber Mode Version 2 (DSMv2), page 5. Added section 3.1 DSMv2 Over EEPROM-Less Application Notes, page 6.

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1. Introduction

This application note will help board layer designers to implement the Deep Slumber Mode (DSM) power saving feature for Realtek's Ethernet Controllers.

For Deep Slumber Mode version 1 (DSMv1), please read the following sections. For Deep Slumber Mode version 2 (DSMv2), go to section 3, page 5.

2. Deep Slumber Mode Version 1 (DSMv1)

When DSMv1 is implemented, the BIOS must enable the DSM_en bit (Set I/O Register Offset 0x6D Bit7 to 1h) **before** the local machine enters the Windows system, and must follow the steps given below **after** the local machine enters the Windows system.

- The board designer must provide a circuit to connect the output GPIO pin. The BIOS then monitors the edge status of output GPIO to determine whether a cable is connected.
- When a cable is unplugged, the output GPIO will go from high to low. The BIOS must set configuration space offset 0x44 to 03h first (the Ethernet Controller enters D3 state), cut off VCC33 (see Figure 1 to Figure 4), and ask the local machine's OS to run a Hardware Scan, which will then remove the Ethernet Controller.
- On connection of a cable, the output GPIO will go from low to high. The BIOS must provide VCC33 and (after 100ms) ask the local machine's OS to run a Hardware Scan in order to recover all resources (E.g., IO space and Memory address). The system is then restored to a normal state.
- When DSM is disabled, the BIOS must disable DSM_en bit (Set I/O Register Offset 0x6D Bit7 to 0h).

Note 1: If Deep Slumber Mode v1 is enabled and the network cable is unplugged, and the OS then enters S3, S4, or S5 power states, the Ethernet Controller will not support Wake-on-LAN (WOL).

Note 2: If implementing EEPROM_Less and DSMv1 Modes at the same time, the BIOS must provide the SVID, SDID, and the Serial Number to the Realtek Ethernet IC after ISOLATEB goes from low to high.

Note 3: If the system does not provide auxiliary power to the Realtek Ethernet IC in S3/S4 states, the BIOS must enable DSM_en again when the system resumes from S3/S4 state.

Note 4: When DSMv1 mode is implemented, the BIOS might declare _RMV code in the ACPI. Refer to section 4 ACPI RMV, page 8. for more details.

Note 5: When DSMv1 mode is implemented, please use the recommended driver revision:

Windows Vista: 6.205 or later

Windows XP: 5.688 or later

Note 6: If the board designer wants to use ISOLATEB to disable the Ethernet Controller, follow the steps below:

Step 1. Set I/O Register Offset 0x6E Bit0 to 0h.

Step 2. Set I/O register Offset 0x6F Bit7 to 0h.

Step 3. Set configuration space offset 0x44 to 03h (the Ethernet Controller enters D3 state).

Step 4. Cut-off VCC33 (see Figure 1 to Figure 4).

Step 5. If the board designer wants to enable the Ethernet Controller, provide VCC33 and set I/O register Offset 0x6F Bit7 to 1h.

2.1. RTL8111C(P) & RTL8111D Output GPIO and ISOLATEB Circuit (64-Pin)

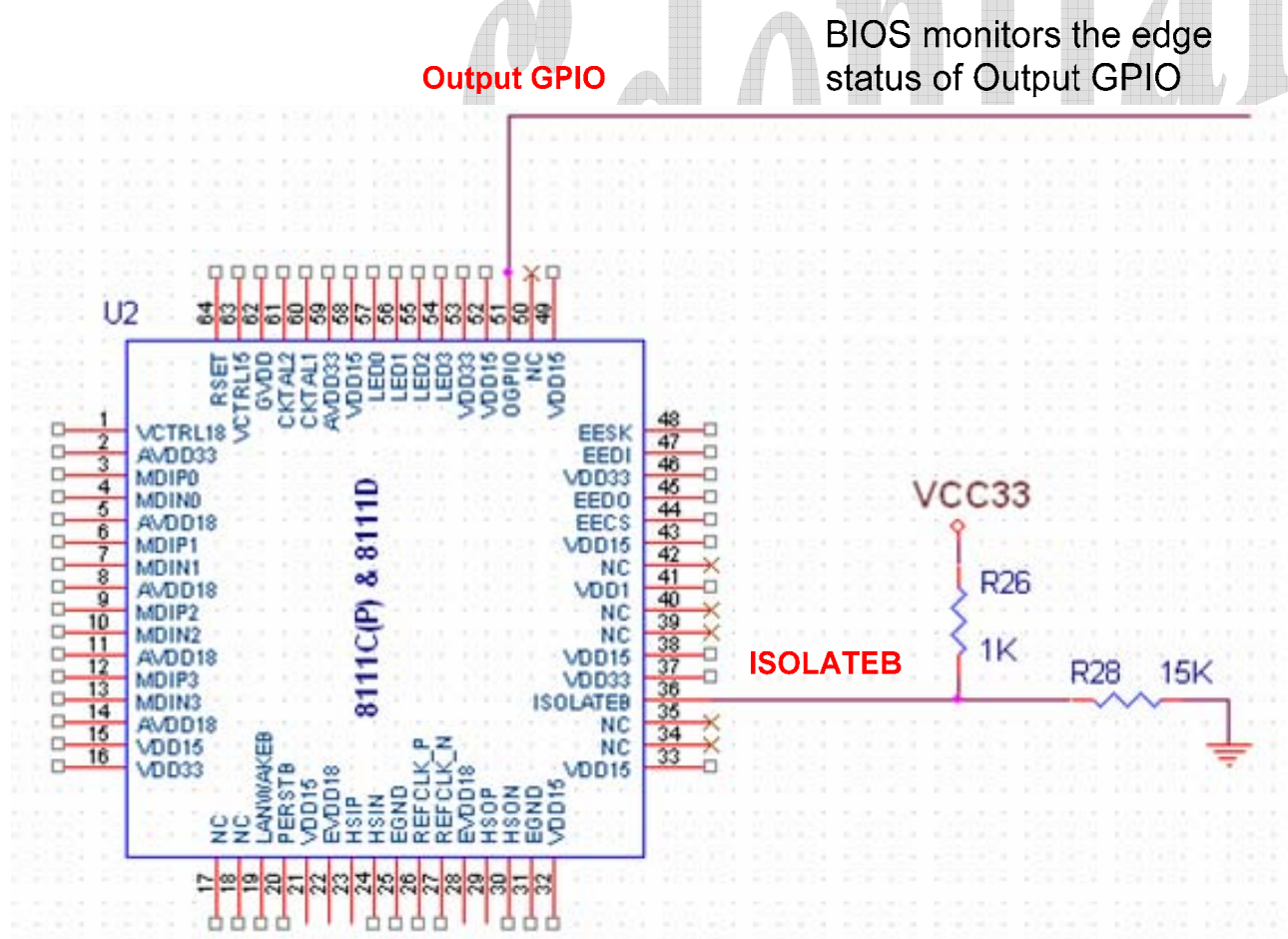


Figure 1. RTL8111C(P) & RTL8111D Output GPIO and ISOLATEB Circuit (64-Pin)

2.2. RTL8103E Output GPIO and ISOLATEB Circuit (64-Pin)

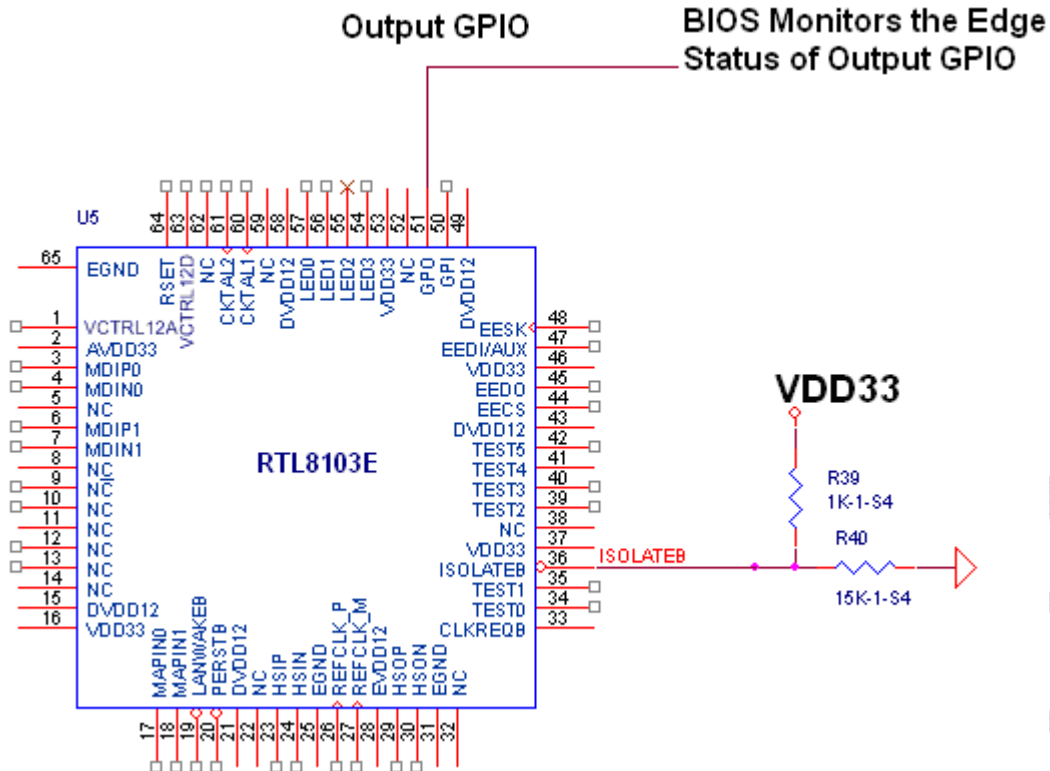


Figure 2. RTL8103E Output GPIO and ISOLATEB Circuit (64-Pin)

2.3. Output GPIO and ISOLATEB Circuit (48-Pin)

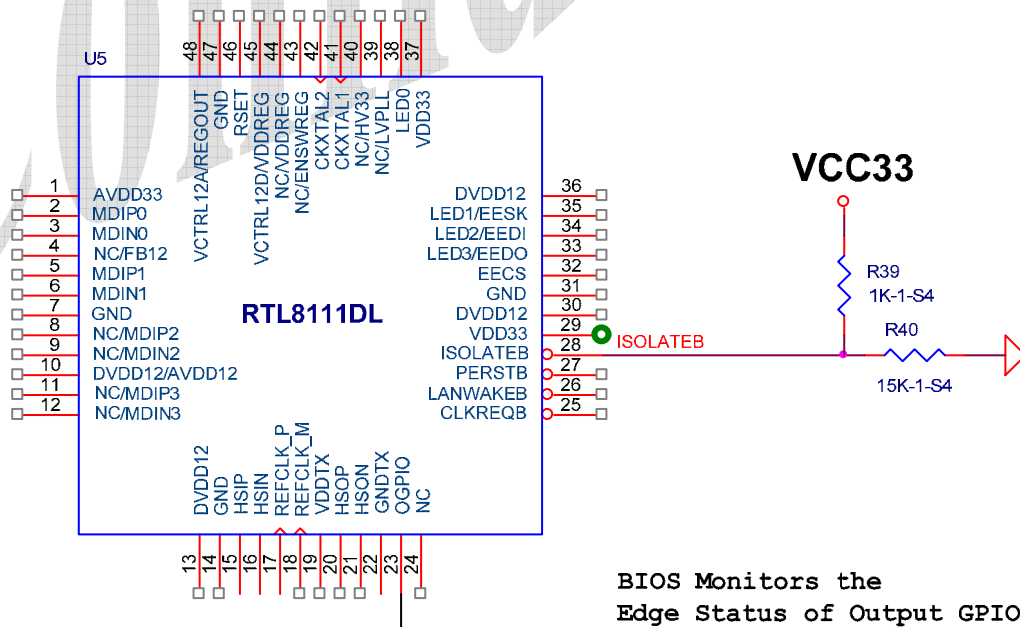


Figure 3. Output GPIO and ISOLATEB Circuit (48-Pin)

2.4. RTL8103T GPO and ISOLATEB Circuit (32-Pin)

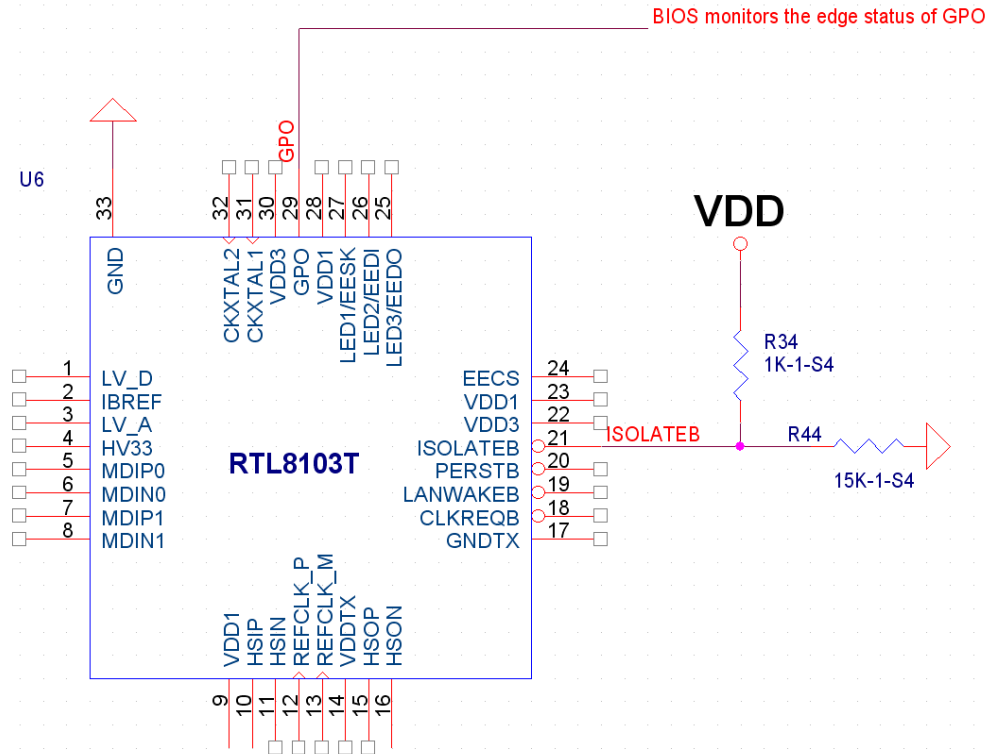


Figure 4. RTL8103T GPO and ISOLATEB Circuit (32-Pin)

2.5. Deep Slumber Mode Version 1 Operation

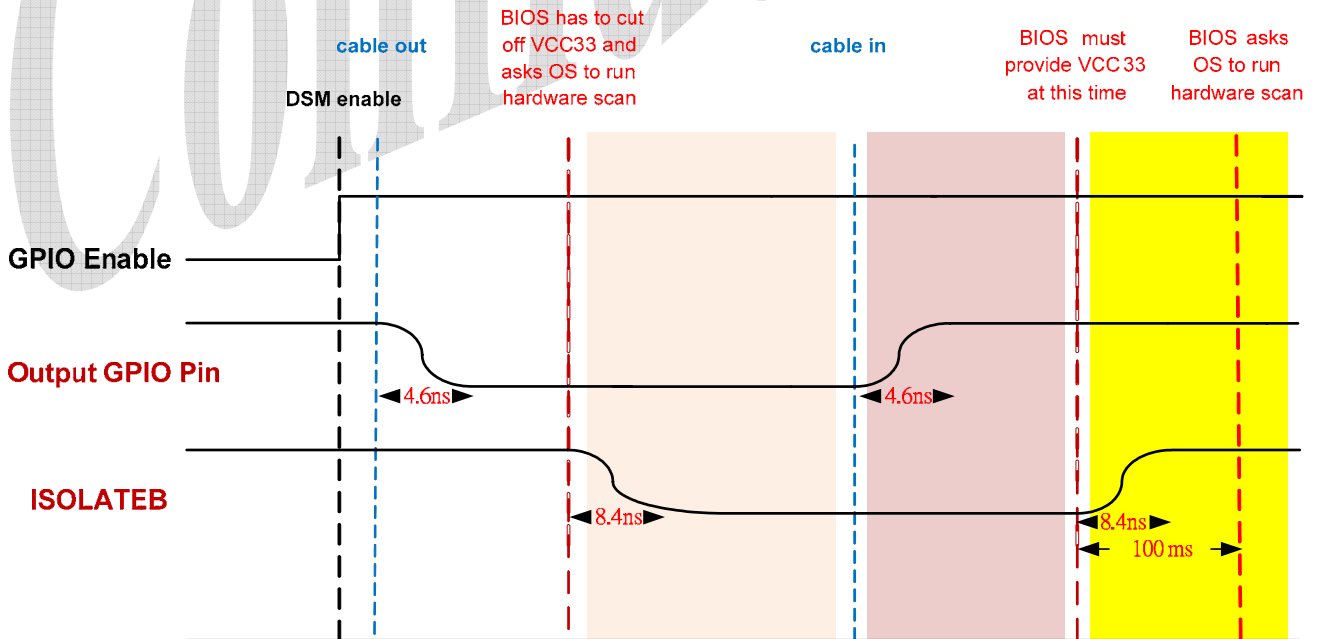


Figure 5. Deep Slumber Mode Version 1 Operation

3. Deep Slumber Mode Version 2 (DSMv2)

Deep Slumber Mode version 2 (DSMv2) is a simplified implementation of DSMv1 that requires very little BIOS effort to implement. The concept is to declare the LAN device as a Hot Plug Device in the BIOS. When a cable is un-plugged, the South Bridge will then detect the Ethernet Controller PCIe connection has disappeared, and the PCIe hot bridge issues an SCI interrupt to execute the Hot Plug ASL code on the specific PCIe port that originally performed the hardware scan and resource allocation. If the hardware scan fails to find the Ethernet Controller, then the OS will remove the Ethernet Controller.

When a cable is plugged-in, the South Bridge will detect that the Ethernet Controller PCIe connection has been recovered, and the Hot Plug mechanism will recover the functionality of the LAN device by performing a hardware scan and re-assigning the required resources (e.g., IO and Memory base addresses), as defined in ASL code.

When DSMv2 is implemented, the BIOS must set following registers in the PCIe host bridge.

- Set Attention Button Pressed (bit0) = 1'b and Presence Detect Changed (bit3) = 1'b in the Slot Status register
- Set Attention Button Pressed Enable (bit0) = 1'b, Presence Detect Changed Enable (bit3) = 1'b, and Hot Plug Interrupt Enable (bit5) = 0'b in the Slot Control register
- Set Hot Plug SCI Enable (HPCE, bit30) = 1'b and Hot Plug SMI Enable (HPME, bit1) = 0'b in the Misc Port Config register at PCIe config space offset D8h
- Clear HOT_PLUG_STS (bit1) in the GPE0 register (PMBase+20h) by writing 1
- Set Uncorrectable Error Mask register (bit14) at offset 148h to mask the reporting of Completion Timeout (CT) errors
- Enable the DSMv2_en bit (set I/O Register Offset 0x6D Bit5 to 1h) *before* the local machine enters the Windows system
- When DSMv2 is disabled, the BIOS must disable the DSMv2_en bit (set I/O Register Offset 0x6D Bit5 to 0h)

Note 1: The chipset (South Bridge) must have the capability to detect the PCIE Ethernet Controller when the Hot Plug function is declared by the BIOS (e.g., in an Intel chipset). Alternatively, the board designer might provide a circuit to connect the output GPIO pin and monitor the edge status of the output GPIO in order to determine whether a cable is connected (e.g., in an AMD chipset).

Note 2: If Deep Slumber Mode v2 is enabled and the network cable is unplugged, and the OS then enters S3, S4, or S5 power states, the Ethernet Controller will not support Wake-on-LAN (WOL).

Note 3: If implementing EEPROM_Less and DSMv2 Modes at the same time, the BIOS must provide the SVID, SDID, and the Serial Number to the Realtek Ethernet IC after the Ethernet connection is made (i.e., a cable is plugged in).

Note 4: If the system does not provide auxiliary power to the Realtek Ethernet IC in S3/S4 states, the BIOS must enable DSMv2_en again when the system resumes from S3/S4 state.

Note 5: When DSMv2 mode is implemented, the BIOS might declare RMV code in the ACPI. Refer to section 4 ACPI RMV, page 8. for more details.

Note 6: When DSMv2 mode is implemented, please use the recommended OS revisions:

For RTL8111D(L)-VB

Windows Vista: 6.218 or later

Windows XP: 5.718 or later

For RTL8103E(L)-VB

Windows Vista: 6.224 or later

Windows XP: 5.730 or later

3.1. DSMv2 Over EEPROM-Less Application Notes

3.1.1. Design Considerations

Several major points must be considered when designing an EEPROM-less feature for Realtek's single-chip Ethernet controller. Those points have been listed below and are detailed in the following sections.

- LAN MAC Address Programming
- DID/VID Programming (if necessary)
- SDID/SVID Programming (if necessary)

3.1.2. LAN MAC Address Programming

Due to the EEPROM-less design goal, the LAN MAC address cannot be loaded from EEPROM and stored in the LAN chip. The BIOS must provide the MAC address to the LAN chip each boot time. The LAN chip will hold the MAC address until AC power off (pulling PCI reset low will not release the MAC address).

If the MAC address is 001122334455h:

Step1: Write C0h to I/O register offset 0x50 by byte access to disable 'register protection'

Step2: Write 33221100h to I/O register offset 0x00 via double word access

Step3: Write 00005544h to I/O register offset 0x04 via double word access

Step4: Write 00h to I/O register offset 0x50 via byte access to enable 'register protection'

3.1.3. DID/VID Programming (If Necessary)

The default DID/VID value of the LAN chip is 8136/10EC. If the board layer designer wants to change the value, follow the steps below:

If VID=10ECh, DID=8136h:

Step1: Write the 813610EC h to I/O register offset 0x64 via double word access

Step2: Write the 8000F000h to I/O register offset 0x68 via double word access

Step3: Wait for 1ms

3.1.4. SID/SVID Programming (If Necessary)

The default SID/SVID value of the LAN chip is 8136/10EC. If the board layer designer wants to change the value, follow the steps below:

If SVID=10ECh, SID=8136h

Step1: Write the 813610ECh to I/O register offset 0x64 via double word access.

Step2: Write the 8000F02Ch to I/O register offset 0x68 via double word access.

Step3: Wait for 1ms.

4. ACPI RMV

The Deep Slumber Mode (DSM) function is a special application of Realtek's Ethernet Controllers. When a cable is unplugged, this function will reduce the power consumption of the system. DSM needs to cooperate with the BIOS and OS. If the BIOS declares RMV code in ACPI to implement DSM mode, the OS will show a 'safely remove hardware' icon in the taskbar, however, the LAN device is not hot-pluggable, and cannot be removed safely using this icon.

If the BIOS does not declare RMV code in ACPI, the OS will not show the 'safely remove hardware' icon. When a cable is disconnected, an error message is entered in the system event log.

Windows Vista System

The Windows Vista system CAN declare `surprise_remove_ok` to avoid multiple error messages in the system event log, but the first error message is unavoidable. The error message has no affect on function. If this error message does not need not to be entered in the event log, declare RMV code in ACPI via the BIOS.

Windows XP System

The Windows XP system CANNOT declare `surprise_remove_ok`. The BIOS might need to define RMV code in the ACPI (a 'safely remove NIC' icon (hot plug device) will be in the taskbar), otherwise an error message will appear.

5. Power Consumption

Measured values from the Realtek demo board are under ASPM L1, CLK_REQ, no EEPROM, and the driver version of Windows XP is version 5.718.

5.1. RTL811C(P) Power Consumption

Table 1. RTL811C(P) Power Consumption

State	Current (mA)	Power (mW)
Normal (Cable Connected, GBE idle)	202.1	667
Link Down Power Saving	77.8	257
Deep Slumber Mode (DSMv1)	26.9	89

5.2. RTL811D(L) Power Consumption

Table 2. RTL811D(L) Power Consumption

State	Current (mA)	Power (mW)
Normal (Cable Connected, GBE idle)	144.8	477.8
Link Down Power Saving	30.6	101
Deep Slumber Mode (DSMv1)	10	33

5.3. RTL811D(L)-VB Power Consumption

Table 3. RTL811D(L)-VB Power Consumption

State	Current (mA)	Power (mW)
Normal (Cable Connected, GBE idle)	144.8	477.8
Advanced Link Down Power Saving	15.5	51.2
Deep Slumber Mode (DSMv2)	9	29.7

5.4. RTL8103E & RTL8103T Power Consumption

Table 4. RTL8103E & RTL8103T Power Consumption

State	Current (mA)	Power (mW)
Normal (Cable Connected, 100M idle)	88	290.4
Link Down Power Saving	50	165
Deep Slumber Mode (DSMv1)	19	62.7

5.5. RTL8103E(L)-VB & RTL8103T-VB Power Consumption

Table 5. RTL8103E(L)-VB & RTL8103T-VB Power Consumption

State	Current (mA)	Power (mW)
Normal (Cable Connected, 100M idle)	88	290.4
Advanced Link Down Power Saving	46	151.8
Deep Slumber Mode (DSMv2)	16	52.8

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